

IN THE CLAIMS:

1. (Original) A method of manufacturing a semiconductor, the method comprising:
forming gate lines on a semiconductor substrate;
forming a first insulating layer between the gate lines;
forming first contact pads and second contact pads in the first insulating layer and
between the gate lines, the first and second contact pads a surface of the semiconductor substrate;
forming a second insulating layer overlying the first and second contact pads;
forming bit lines on the second insulating layer, the bit lines electrically connected to the
second contact pads and extending across the gate lines;
forming a third insulating layer overlying the bit lines; and
forming band-type openings by selectively etching a portion of the third insulating layer,
wherein the band-type openings extend in a lengthwise direction of the gate lines to expose the
first contact pads, and wherein the band-type openings have portions that protrude in a
lengthwise direction of the bit lines.
2. (Original) The method of claim 1, further comprising:
forming a conductive layer on the third insulating layer, wherein the conductive layer fills
the band-type openings and is electrically connected to the first contact pads;
separating the conductive layer into individual storage node contact bodies; and
forming storage nodes on the storage node contact bodies.
3. (Original) The method of claim 1, wherein the protruding portions are positioned
between the bit lines.
4. (Original) The method of claim 3, wherein the protruding portions comprise a
triangular with vertices disposed between the bit lines.
5. (Original) The method of claim 1, wherein the protruding portions comprise
adjacent protruding portions protrude in opposite directions and each bit lines is positioned
between the adjacent protruding portions.

6. (Original) The method of claim 1, wherein the openings has a bottom portion with a line width less than a line width of an upper portion of the openings so as to have oblique sidewalls.

7. (Original) The method of claim 6, wherein the upper portion of the openings overlaps an upper portion of the gate lines at the protruding portions.

8. (Original) The method of claim 6, wherein the upper portion of the openings partially overlaps an upper portion of the second contact pads at the protruding portions.

9. (Original) The method of claim 6, wherein forming band-type openings comprises taper etching to make the sidewalls of the openings oblique.

10. (Original) The method of claim 1, wherein forming band-type openings comprises forming band-type openings that extend across and expose the bit lines.

11. (Original) The method of claim 1, further comprising:
forming a capping insulating layer overlying the bit lines; and
forming spacers to cover the sidewalls of the bit lines.

12. (Original) The method of claim 11, further comprising forming a conductive layer on the third insulating layer, wherein the conductive layer fills the band-type openings and is electrically connected to the first contact pads, wherein forming the conductive layer comprises planarizing the conductive layer until the upper surface of the capping insulating layer is exposed.

13. (Original) A method of manufacturing a semiconductor device, the method comprising:
forming gate lines on a semiconductor substrate;
forming a first insulating layer between the gate lines;

forming first contact pads and second contact pads between the gate lines and in the first insulating layer to be electrically connected to a surface of the semiconductor substrate; forming a second insulating layer overlying the first and second contact pads; forming bit lines on the second insulating layer, the bit lines extending across the gate lines and electrically connected to the second contact pads through the second insulating layer; forming a third insulating layer overlying the bit lines; forming zigzag-shaped band-type openings by selectively etching a portion of the third insulating layer, wherein the band-type openings extend in a lengthwise direction of the gate lines to expose the first contact pads; forming a conductive layer on the third insulating layer to fill the band-type openings, the conductive layer electrically connected to the first contact pads; separating the conductive layer into individual storage node contact bodies; and forming storage nodes on the storage node contact bodies.

14. [[13.]] (Currently Amended) The method of claim 13 [[12]], wherein the band-type openings have a pair of a protruding portion and a concave portion, in a lengthwise direction of the bit lines, the protruding portion facing the concave portion between the bit lines.

15. [[14.]] (Currently Amended) The method of claim 13 [[12]], wherein forming band-type openings comprises forming band-type openings that are serpentine in shape, wherein an outermost and innermost edge of the band-type openings are positioned between the bit lines.

16. [[15.]] (Currently Amended) The method of claim 13 [[12]], wherein the openings has a bottom portion with a line width that is less than a line width of an upper portion of the openings so as to have oblique sidewalls.

17. [[16.]] (Currently Amended) The method of claim 16 [[15]], wherein the openings extend such that the upper portion of the openings overlaps an upper portion of the gate lines at the protruding portions.

18. [[17.]] (Currently Amended) The method of claim 16 [[15]], wherein the openings extend such that the upper portion of the openings partially overlaps an upper portion of the second contact pads, between which each gate line is positioned, at the protruding portions.

19. [[18.]] (Currently Amended) The method of claim 16 [[15]], wherein forming band-type openings comprises using taper etching to make the sidewalls of the openings oblique.

20. [[19.]] (Currently Amended) The method of claim 13 [[12]], further comprising: forming a capping insulating layer to cover the bit lines; and forming spacers to cover the sidewalls of the bit lines.

21. [[20.]] (Currently Amended) The method of claim 20 [[19]], wherein forming the conductive layer comprises planarizing the conductive layer until the upper surface of the capping insulating layer is exposed.

22. [[21.]] (Currently Amended) The method of claim 13 [[12]], wherein forming storage nodes on the storage node contact bodies comprises forming adjacent storage nodes, between which each bit line is positioned, the storage nodes arranged in a direction diagonal to the lengthwise direction of the bit line.

23. [[22.]] (Currently Amended) The method of claim 13 [[12]], wherein the storage nodes are formed in the shape of cylinders having circular or rectangular areas.

24. [[23.]] (Currently Amended) The method of claim 23 [[22]], further comprising forming a buffer layer to cover lower sides of the cylindrical storage nodes.*

25. [[24.]] (Currently Amended) The method of claim 13 [[12]], wherein an edge-to-edge width of the band-type openings is constant, and wherein a position of the edges of the band-type openings varies along the lengthwise direction of the gate lines.